

1 SYNCHRONIZATION OF TWO OR
2 MORE VIDEO PLAYERS

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4 BACKGROUND OF THE INVENTION

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6 This invention relates to a synchronizer for synchronous recovery
7 of video signals from two or more video players, and to a video player
8 system incorporating such a synchronizer in addition to two or more video
9 players and one or more displays.

10 By the term "video player," as used herein and in the claims
11 appended hereto, is meant a player, with or without recording facilities,
12 of any video storage media, such as those in tape form, as in the case
13 of a video tape recorder (VTR), and in disk form, as in the case of a
14 videodisk player as typified by a digital versatile disk (DVD) player.
15 The invention is applicable to any such video players as well as to a
16 system of two or more such video players together with one or more
17 displays.

18 It has been known and practiced conventionally to synchronously
19 drive two or more VTRs, for example, for simultaneous reproduction of as
20 many correlated video signals on separate displays or on separate sections
21 or windows of one display screen. Japanese Unexamined Patent Publica-
22 tion No. 52-56513 to Matsushita Electric is hereby cited as describing and
23 claiming how to synchronize two or more video VTRs for use with video
24 tapes having longitudinal picture and sound tracks. Essentially, it teaches
25 to compare the phases of the vertical synchronizing pulses, included in
26 the recovered video signals, with that of a series of reference pulses
27 from a source external to the tapes or to the VTRs. The drive motors
28 for the rotary drums carrying the magnetic heads, or those for the cap-
29 stans, of both VTRs are controlled so as to keep the vertical sync pulses
30 of the video signals being reproduced, in phase with the external refer-
31 ence pulses.

32 An objection to this prior art method is that it necessitates the
33 provision of a source of accurately timed reference pulses. Such a pulse
34 source is costly and would make the resulting synchronizer significantly
35 more expensive than in the absence thereof.

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1 tical sync pulses, the play synchronization will then a first and a second
2 phase departure signal for the first and the second series of vertical
3 sync pulses. The first phase departure signal will now contain no signif-
4 icant pulse because the reference moment has been determined to be at
5 the trailing edge of each vertical sync pulse of the first series. The
6 second phase departure signal will do, however, contain a pulse having a
7 duration in proportion to the phase departure of each vertical sync pulse
8 of the second series. This second phase departure signal is utilized, for
9 example, to accelerate the capstan motor of the first video player into
10 phase with the second.

11 It is thus seen that the invention dispenses with a dedicated
12 source of timing pulses for phase comparison of the two or more series
13 of vertical sync pulses. The synchronizer according to the invention is
14 therefore manufacturable much more inexpensively than the conventional
15 devices incorporating such reference pulse sources.

16 The above and other objects, features and advantages of the in-
17 vention and the manner of realizing them will become more apparent, and
18 the invention itself will best be understood, from the following description
19 taken together with the attached drawings showing the preferred embodi-
20 ments of the invention.

21 22 *BRIEF DESCRIPTION OF THE DRAWINGS*

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24 FIG. 1 is a block diagram showing the synchronizer according to
25 the present invention as incorporated in a two-VTR, two-display system
26 by way of one possible application of the invention;

27 FIG. 2 is a schematic diagram, partly in block form, showing in
28 more detail the two VTRs of the FIG. 1 embodiment together with the
29 synchronizer according to the invention;

30 FIG. 3 is a block diagram showing those functional means in the
31 controller of one of the two VTRs of FIG. 2 which have relevance to
32 the synchronizer according to the invention, the controller of the other
33 VTR being of identical design;

34 FIG. 4 is a block diagram showing in some more detail the syn-
35 chronizer of the FIG. 1 embodiment together with those parts of the
36 VTRs which are directly associated with the synchronizer;

1 FIG. 5 is a schematic electrical diagram, partly in block form, of
2 the play synchronization circuit of the FIG. 4 synchronizer;

3 FIG. 6 is a schematic electrical diagram of the VTR status judg-
4 ment circuit included in the FIG. 5 play synchronization circuit;

5 FIG. 7 is a diagram of waveforms of signals appearing in various
6 parts of the FIG. 5 play synchronization circuit during compulsory syn-
7 chronization of the two FIG. 1 VTRs in the case where no phase differ-
8 ence exists between the two series of vertical sync pulses from the
9 VTRs;

10 FIG. 8 is a waveform diagram similar to FIG. 7 but showing the
11 same signals in the case where the first series of vertical sync pulses,
12 from one of the two FIG. 1 VTRs, are delayed in phase from the second
13 series of such pulses from the other VTR;

14 FIG. 9 is also a waveform diagram similar to FIG. 7 but showing
15 the same signals in the case where the second series of vertical sync
16 pulses are delayed in phase from the first series of such pulses;

17 FIG. 10 is a block diagram of a three-VTR, three-display video
18 player system employing the synchronizer according to the invention;

19 FIG. 11 is a somewhat more detailed block diagram of the synchro-
20 nizer of the FIG. 10 embodiment, shown together with some pertinent out-
21 put and input terminals of the three VTRs;

22 FIG. 12 is a schematic electrical diagram of the play synchroniza-
23 tion circuit of the FIG. 11 synchronizer;

24 FIG. 13 is a diagram of waveforms of signals appearing in var-
25 ious parts of the FIG. 12 play synchronization circuit during compulsory
26 synchronization of the three FIG. 10 VTRs in the case where no phase
27 difference exists between the three series of vertical sync pulses from
28 the VTRs;

29 FIG. 14 is a waveform diagram similar to FIG. 13 but showing the
30 same signals in the case where the three series of vertical sync pulses,
31 from the three FIG. 10 VTRs, all differ in phase from one another;

32 FIG. 15 is also a waveform diagram similar to FIG. 13 but showing
33 the same signals in the case where a phase difference exists between the
34 first and the third series of vertical sync pulses and where the second
35 of the three FIG. 10 VTRs is not in play mode;

36 FIG. 16 is a schematic electrical diagram of a slight modification of

1 the FIG. 5 play synchronization circuit;

2 FIG. 17 is a schematic electrical diagram of a slight modification of
3 the FIG. 12 play synchronization circuit; and

4 FIG. 18 is a partial schematic electrical diagram of an additional
5 slight modification of the play synchronization circuit according to the
6 invention.

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8 *DESCRIPTION OF THE PREFERRED EMBODIMENTS*

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10 The present invention will now be described in detail as applied
11 by way of example to the two-VTR, two-display video player system il-
12 lustrated in FIG. 1. The exemplified video player system has a first 1a
13 and a second 1b VTR of like design, a first 2a and a second 2b display
14 which also are of identical make, and a play synchronizer 3 forming the
15 gist of the invention. The VTRs 1a and 1b are both conventionally
16 equipped to record composite video signals, including picture signals as
17 well as synchronizing and blanking pulses, on magnetic tapes in cassette
18 form, not shown in this figure, and later reproduce and send them to the
19 displays 2a and 2b, respectively, for visual presentation of two correlated
20 pictures. Alternatively, the video signals from both VTRs may be direct-
21 ed into one display, as indicated by the broken-line arrow in this figure,
22 for reproduction of the two pictures on separate parts or windows of the
23 same screen.

24 The play synchronizer 3 is shown connected to both VTRs 1a and
25 1b as a synchronization adapter, so to say, for compulsorily synchronizing
26 them during playback operation by deriving the series of standard vertical
27 sync pulses from the composite video signals being recovered from the
28 commercially available tape cassettes by both VTRs. Relying on these
29 vertical sync pulses, the play synchronizer 3 produces what are herein
30 termed phase departure signals, which are directed back into both VTRs
31 for compulsorily synchronizing them as manifested by the phasing of the
32 all the series of vertical sync pulses.

33 Reference may be had to FIG. 2 for more detailed study of the
34 VTRs 1a and 1b. Since the two VTRs are of similar construction, like
35 reference numerals will be used to denote like parts of both devices, as
36 well as of the tape cassettes shown loaded therein, only with the letters

1 a and b suffixed to such numerals to denote which VTR the parts be-
2 long to. Only the first VTR 1a will be detailed, it being understood
3 that the same description applies to the second 1b

4 Essentially constructed according to the standard VHS design, the
5 representative VTR 1a is for use with a commercially available video tape
6 cassette 4a wherein a length of magnetic tape 7a has its opposite extrem-
7 ities anchored to a pair of reels 5a and 6a to run bidirectionally there-
8 between. It is understood that a video signal is recorded on the tape
9 7a along a series of slanting tracks in conformity with, for example, the
10 NTSC or PAL standards. As is well known, the standard video signal in-
11 cludes the vertical sync pulses, in addition to the visual information, that
12 are transmitted at the end of each field to keep the receiver in
13 field-by-field synchronism with the transmitter. The picture is blanked
14 during each vertical retrace period, when the electron beam is returned
15 to the top of the screen at the end of one field. The tape 7a has also
16 a control signal recorded longitudinally thereon.

17 Pulled out the cassette 4a and guided by guide pins, the tape 7a
18 is wrapped a required angle over a rotary drum 8a to which a pair of
19 magnetic read/write heads or transducers 8a and 9a are mounted in dia-
20 metrically opposite positions thereon. The tape 7a is wound on the drum
21 8a at such an angle to its axis as to enable the transducers to trace
22 the slanting tracks thereon. A drum motor 11a is drivingly coupled to
23 the drum 8a. It is to be understood that the transducers 8a and 9a as
24 well as their electrical connections are shown highly schematically in FIG.
25 2 by way of illustration and explanation.

26 Along the tape path from one reel to the other of the cassette 4a
27 there are sequentially arranged a control head 12a, an audio head, not
28 shown, an erase head, also not shown, and a cooperative combination of
29 capstan 13a and pinch roller 14a. A capstan motor 15a is drivingly cou-
30 pled to the capstan 13a for constant speed tape travel. Tachometers 16a
31 and 17a are coupled to the drum motor 11a and capstan motor 15a, respec-
32 tively, for feedback speed control of the motors. The drum 8a carries in
33 a prescribed position on its circumference a part 18a to be sensed or
34 detected by a head or detector 19a for switching between the transducers
35 8a and 9a.

36 Also included in the representative VTR 1a are a tape transport

1 20a, a signal processing network 21a, a controller 22a, a drum motor driv-
2 er circuit 23a, and a capstan motor driver circuit 24a. Drivingly coupled
3 to the cassette reels 5a and 6a, tape transport 20a operates under the
4 direction of the controller 22a for causing bidirectional tape travel there-
5 between.

6 The signal processing network 21a is electrically connected to the
7 pair of transducers 9a and 10a on the drum 8a for conventionally process-
8 ing the video signals recovered from the tape and those to be recorded
9 thereon. More specifically, the network 21a comprises a transducer switch-
10 ing circuit, a video amplifier, and a frequency-demodulator for processing
11 the signals recovered, and a frequency-modulator and a recording amplifier
12 for processing the signals to be recorded. The network 21a is shown
13 connected to two video output terminals 25a and 26a for production of
14 the video signals.

15 The controller 22a is connected to all of the control head 12a,
16 tachometers 16a and 17a, transducer switching position detector 19a, tape
17 transport 20a, signal processing network 21a, drum motor driver circuit
18 23a, and capstan motor driver circuit 24a, as well as to the play syn-
19 chronizer 3 which is external to the VTR 1a. The controller 22a is per-
20 se of conventional make including a microprocessor for performing a varie-
21 ty of control functions.

22 For the purposes of this invention, however, the controller 22a
23 may be considered comprising the means depicted block-diagrammatically in
24 FIG. 3; namely, a drum motor servo circuit 31a, a tape transport control
25 circuit 32a, a signal processing network control circuit 33a, a capstan
26 motor servo circuit 34a, a play command circuit 35a, a tape-end detector
27 circuit 36a, and a sync pulse separation control circuit 37a.

28 The drum motor servo circuit 31a has an input connected to the
29 transducer switching position detector 19a, and another input to the drum
30 motor tachometer 16a, both shown in FIG. 2, for producing a control sig-
31 nal for the drum motor 11a in response to the outputs therefrom. The
32 control signal is delivered to the drum motor driver circuit 23a, FIG. 2.

33 The tape transport control circuit 32a controls the tape transport
34 20a, FIG. 2. The signal processing network control circuit 33a controls
35 the signal processing network 21a, FIG. 2.

36 The capstan motor servo circuit 34a has an input connected to

1 the control head 12a, and another input to the tachometer 17a, both
2 shown in FIG. 2, for producing a tape speed control signal for causing
3 the capstan motor 15a to drive the tape 7a at a required speed. The
4 tape speed control signal is supplied to the capstan motor driver circuit
5 24a, as well as to the play synchronizer 3 by way of a first controller
6 output terminal 38a.

7 The play command circuit 35a responds to the actuation of a play
8 switch, not shown, by the user by delivering a play command to the play
9 synchronizer 3 from a second controller output terminal 39a. The play
10 command is of course utilized internally of the VTR 1a, too, by means
11 that are not shown because of impertinence to the invention.

12 The tape-end detector circuit 36a has an output connected to a
13 third controller output terminal 40a for providing a signal indicative of
14 whether the tape has been run to the predetermined end of the tape
15 (EOT). The EOT signal is also delivered to the play synchronizer 3 from
16 the third controller output terminal 40a.

17 The sync pulse separation control circuit 37a has an output con-
18 nected to a fourth controller output terminal 41a for providing a control
19 signal for separation of the vertical sync pulses from the recovered video
20 signal. This control signal is also fed to the play synchronizer 3 from
21 the fourth controller output terminal 41a.

22 In FIG. 4 is shown in more detail the play synchronizer 3 in
23 combination with some directly associated parts of the VTRs 1a and 1b.
24 The play synchronizer 3 is herein shown, however, only in terms of three
25 component circuits into which it is broadly divisible, more detailed illus-
26 tration being to be presented subsequently. The three constituent cir-
27 cuits are two vertical sync pulse separator circuits 42a and 42b for sepa-
28 ration of the vertical sync pulses from the video signals being recovered
29 from the tapes in the VTRs 1a and 1b, respectively, and a play synchro-
30 nization circuit 43 for production of the play synchronization signals for
31 delivery back to the VTRs.

32 The first vertical sync pulse separator circuit 42a of the play
33 synchronizer 3 has an input connected to the signal processing network
34 21a of the first VTR 1a via the video output 26a, and another input to
35 the sync pulse separation control circuit 37a, FIG. 3, of the controller 22a
36 of the first VTR via the fourth controller output terminal 41a. The sec-

1 ond vertical sync pulse separator circuit 42b of the play synchronizer 3
2 has an input connected to the signal processing network 21b of the sec-
3 ond VTR 1b via the video output 26b, and another input to the sync
4 pulse separation control circuit of the controller 22b of the second VTR
5 via the fourth controller output terminal 41b.

6 So connected to the necessary parts of the VTRs 1a and 1b, the
7 vertical sync pulse separator circuits 42a and 42b derive the vertical
8 sync pulses from the video signals supplied from the VTRs and deliver
9 to the play synchronization circuit 43 one rectangular output pulse per
10 field. The separation of sync pulses from video signals is familiar to
11 television specialists, so that no more detailed illustration or description of
12 the sync pulse separator circuits 42a and 42b is deemed necessary.
13 These circuits 42a and 42b could be built into the VTRs 1a and 1b,
14 respectively.

15 As indicated also in FIG. 4, the play synchronization circuit 43
16 has inputs connected to the two vertical sync pulse separator circuits 42a
17 and 42b by way of lines 44a and 44b, to the first to third controller
18 output terminals 38a, 39b and 40a of the first VTR 1a by way of lines
19 45a, 46a and 47a, and to the first to third controller output terminals
20 38b, 39b and 40b of the second VTR 1b by way of lines 45b, 46b and
21 47b. The play synchronization circuit 43 has two output lines 48a and
22 48b connected to the input terminals 49a and 49b, and thence to the
23 capstan motor driver circuits 24a and 24b, of the VTRs 1a and 1b, re-
24 spectively.

25 Inputting the two vertical sync pulse signals from the separator
26 circuits 42a and 42b, the play synchronization circuit 43 operates to com-
27 pare their phases one with respect to the other. For such phase com-
28 parison this circuit 43 determines a reference moment in prescribed time
29 relationship to each pulse of one of the two input signals and provides
30 phase departure signals indicative of a possible phase departure of each
31 pulse of each input signal with respect to that reference moment. The
32 phase departure signals are delivered one to each VTR for controlling the
33 speeds of the capstan motors 15a and 15b. Since each pulse of said one
34 input signal has no phase departure from the reference moment, only the
35 capstan motor associated with the other input signal has its speed read-
36 justed for synchronizing this other signal with said one.

1 The reader's attention is now invited to FIG. 5 for closer study
2 of the play synchronization circuit 43 of the play synchronizer 3. Broad-
3 ly, the play synchronization circuit 43 comprises a VTR status judgment
4 circuit 50 for ascertaining whether both VTRs 1a and 1b are in condition
5 for compulsory play synchronization according to the invention, a reference
6 moment determination circuit 51 for establishment of a reference moment
7 with respect to each vertical sync pulse of either of the two incoming
8 series of such pulses, two NOT circuits 52 and 53, two D flip-flops 54
9 and 55 as phase comparators for providing the phase departure signals,
10 and two adders 56 and 57.

11 As shown in detail in FIG. 6, the VTR status judgment circuit 50
12 has two NOT circuits 58 and 59, and three AND gates 60, 61 and 62,
13 although these AND gates could be input-inverting NOR gates. The first
14 AND gate 60 has one input connected to the play command circuit 35a,
15 FIG. 3, of the controller 22a of the first VTR 1a by way of the line
16 46a, and another input to the EOT detector circuit 36a, FIG. 3, of the
17 controller 22a via the NOT circuit 58 and by way of the line 47a.
18 Likewise, the second AND gate 61 has one input connected to the equiva-
19 lent of the play command circuit 35a in the controller 22b of the second
20 VTR 1b by way of the line 46b, and another input to the equivalent of
21 the EOT detector circuit 36a in the controller 22b via the NOT circuit
22 59 and by way of the line 47b.

23 The third AND gate 62 of the VTR status judgment circuit 50
24 has its two inputs connected to the first two AND gates 60 and 61.
25 The output of the AND gate 62, and of the complete VTR status judg-
26 ment circuit 50, is connected to the reference moment determination circuit
27 51, FIG. 5, by way of a line 63. It is thus seen that the judgment cir-
28 cuit 50 judges that the VTRs 1a and 1b are in condition for compulsory
29 synchronization when both VTRs are in play mode and, at the same time,
30 when the tapes 7a and 7b are both not driven to their ends. The
31 judgment circuit 50 will go high when all these conditions prove to be
32 met.

33 With reference back to FIG. 5 the reference moment determination
34 circuit 51 of the play synchronization circuit 43 comprises a D flip-flop
35 64, a OR gate 65, a NOR gate 66, a NAND gate 67, and an AND gate
36 68. The OR gate 65 has its two inputs connected to the vertical sync

1 pulse separator circuits 42a and 42b, FIG. 4, by way of the noted input
2 lines 44a and 44b, respectively, and its output to the clock input *T* of
3 the flip-flop 64. This flip-flop 64 will be hereinafter referred to as the
4 reference moment flip-flop in contradistinction from the flip-flops 54 and
5 55 of the play synchronization circuit 43, which will then be referred to
6 as the play synchronization flip-flops.

7 The NOR gate 66 has one input connected to the *Q* output of
8 the play synchronization flip-flop 54, another input to the *Q* output of
9 the other play synchronization flip-flop 55, and an output to the data
10 input *D* of the reference moment flip-flop 64. The NAND gate 67 has
11 its two inputs likewise connected respectively to the *Q* outputs of the
12 play synchronization flip-flops 54 and 55. The AND gate 68 has one
13 input connected to the output line 63 of the VTR status judgment circuit
14 50, another input to the NAND gate 67, and an output to the reset or
15 clear input *R* of the reference moment flip-flop 64. The preset input *PR*
16 of this flip-flop 64 is connected to a positive supply terminal designated
17 *+V*.

18 The play synchronization flip-flop 54 has a trigger input *T* con-
19 nected to the first vertical sync signal input line 44a via the NOT cir-
20 cuit 52, a data input *D* and a preset input *PR* both connected to a
21 positive supply terminal *+V*, and a reset input *R* connected to the *Q* out-
22 put of the reference moment flip-flop 64.

23 The other play synchronization flip-flop 55 has a trigger input *T*
24 connected to the second vertical sync signal input line 44b via the NOT
25 circuit 53, a data input *D* and a preset input *PR* both connected to a
26 positive supply terminal *+V*, and a reset input *R* connected to the *Q* out-
27 put of the reference moment flip-flop 64.

28 Both play synchronization flip-flops 54 and 55 are to be reset
29 when their reset inputs *R* go low. These play synchronization flip-flops
30 are intended as aforesaid for production of phase departure pulses for
31 eliminating a phase differences, if any, between the two series of vertical
32 sync pulses from the VTRs 1a and 1b. Each flip-flop will put out such
33 phase departure pulses during the vertical retrace periods, one pulse for
34 each field.

35 The adder 56 has one input connected to the *Q* output of the
36 play synchronization flip-flop 54, another input connected by way of the

1 line 45b to the equivalent of the capstan motor servo circuit 34a, FIG. 3,
2 in the controller 22b of the second VTR 1b, and an output connected by
3 way of the line 48b to the capstan motor driver circuit 24b, FIGS. 2 and
4 4, of the second VTR 1b. The capstan motor 15b is therefore driven
5 according to the addition of the output from the capstan motor servo cir-
6 cuit in the second VTR controller 22b and the output from the play
7 synchronization flip-flop 54.

8 The other adder 57 has one input connected to the Q output of
9 the other play synchronization flip-flop 55, another input connected by
10 way of the line 45a to the capstan motor servo circuit 34a, FIG. 3, of
11 the controller 22a of the first VTR 1a, and an output connected by way
12 of the line 48a to the capstan motor driver circuit 24a, FIGS. 2 and 4,
13 of the first VTR 1a. The capstan motor 15a is likewise driven according
14 to the addition of the output from the capstan motor servo circuit 34a
15 and the output from the play synchronization flip-flop 55.

16 17 Operation

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19 The operation of the two-VTR video player system, particularly of
20 the play synchronizer 3, constructed as hereinbefore described with refer-
21 ence to FIGS. 1-6, will be best understood by referring to the waveform
22 diagrams of FIG. 7-9. The following indicia will be used to denote some
23 pertinent signals associated with the play synchronizer in the following
24 operational description of the player system:

25 V_{s1} = first series of vertical sync pulses from the first vertical
26 sync pulse separator circuit 42a

27 V_{s2} = second series of vertical sync pulses from the second verti-
28 cal sync pulse separator circuit 42b

29 V_{65} = output from the OR gate 65 of the reference moment de-
30 termination circuit 51

31 V_{64} = output from the play synchronization flip-flop 54, equivalent
32 to the phase departure signal to be applied to the second
33 VTR 1b or the phase difference between the first vertical
34 sync pulses V_{s1} and the output V_{64} of the flip-flop 64

35 V_{66} = output from the other play synchronization flip-flop 55,
36 equivalent to the phase departure signal to be applied to
37 the VTR 1a or the phase difference between the second vertical
38 sync pulses V_{s2} and the output V_{64} of the flip-flop 64

1 V_{64} = output from the reference moment flip flop 64

2 V_{66} = output from the NOR gate 66 of the reference moment de-
3 termination circuit 51

4 V_{67} = output from the NAND gate 67 of the reference moment
5 determination circuit 51

6 V_{68} = output from the AND gate 68 of the reference moment de-
7 termination circuit 51.

8 FIG. 7 represents the foregoing voltage signals appearing in the
9 various parts of the play synchronization circuit 43, FIG. 5, when no
10 phase difference exists between the two series of vertical sync pulses
11 V_{s1} and V_{s2} derived from the video signals from the VTRs 1a and 1b by
12 the sync pulse separator circuits 42a and 42b; FIG. 8 the same voltage
13 signals when the sync pulses V_{s1} from the first VTR lag in phase be-
14 hind the sync pulses V_{s2} from the second VTR; and FIG. 9 the same
15 voltage signals when the sync pulses from the first VTR have a phase
16 advance over those from the second VTR.

17 The VTR status judgment circuit 50, FIG. 6, of the play synchro-
18 nization circuit 43 will go high as aforesaid when both VTRs 1a and 1b
19 are in play mode and, at the same time, when the tapes 7a and 7b are
20 not run to their ends. The reference moment flip-flop 64, FIG. 5, will
21 then be not reset but operate to permit forced synchronization of the
22 two VTRs.

23 On the other hand, when either or both of the VTRs 1a and 1b
24 are not in play mode, or when the tape end is reached in either or
25 both of these VTRs, the VTR status judgment circuit 50 will go low to
26 indicate that the VTRs are not fit for synchronization. The AND gate
27 68, FIG. 5, of the reference moment determination circuit 51 will then also
28 go low, resetting the flip-flop 64 and so making its Q output go low,
29 too. This low output being applied to the reset inputs R of both play
30 synchronization flip-flops 54 and 55, the play synchronization circuit 43
31 will not operate.

32 Incidentally, in the FIG. 5 play synchronization circuit 43, the
33 NAND gate 67 will go low when both flip-flops 54 and 55 go high. The
34 AND gate 68 will then also go low, resetting the reference moment flip-
35 flop 64. The play synchronization flip-flops 54 and 55 will be thereby
36 reset in turn.

1 Let us now assume that the VTRs 1a and 1b are now in condition
2 for compulsory synchronization according to the invention. Supplied from
3 the vertical sync pulse separator circuits 42a and 42b, FIG. 4, over their
4 output lines 44a and 44b, the sync pulses V_{s1} and V_{s2} will be inverted
5 in polarity by the NOT circuits 52 and 53 before being applied to the
6 clock inputs of the play synchronization flip-flops 54 and 55, respectively.
7 These flip-flops 54 and 55 will take in the high input to their data in-
8 put terminals D at the moments of the trailing edges of the incoming
9 vertical sync pulses, that is, of the rises of the outputs from the NOT
10 circuits 52 and 53. However, being under the control of the reference
11 moment flip-flop 64, the play synchronization flip-flops 54 and 55 will not
12 remain set for any significant period of time, as will become better un-
13 derstood as the description proceeds.

14 If then the series of vertical sync pulses V_{s1} and V_{s2} from both
15 VTRs 1a and 1b are in phase with each other as has been assumed
16 above in conjunction with FIG. 7, the output pulses V_{65} of the OR gate
17 65, FIG. 5, will also be in phase with these vertical sync pulses.
18 Clocked by the leading edges of these OR gate output pulses V_{65} , the
19 reference moment flip-flop 64 will take in the output V_{66} from the NOR
20 gate 66 through its data input D . The NOR gate output V_{66} is shown
21 in FIG. 7 to be high (H) at t_1 when the outputs V_{54} and V_{55} from the
22 play synchronization flip-flops 54 and 55 are both low (0). Consequently,
23 the output V_{64} from the reference moment flip-flop 64 will go high at t_1
24 at the moment of the leading edge of the output pulse V_{65} of the OR
25 gate 65. Thus the play synchronization flip-flops 54 and 55 will both
26 become operable at t_1 .

27 Then, clocked at t_2 by the trailing edges of the vertical sync
28 pulses V_{s1} and V_{s2} , or by the rises of the outputs from the NOT cir-
29 cuits 52 and 53, the play synchronization flip-flops 54 and 55 will take
30 in their data inputs D . The play synchronization flip-flop outputs V_{54}
31 and V_{55} will thus go high at t_2 . The output V_{67} from the NAND gate
32 67 of the reference moment determination circuit 51 will go low in re-
33 sponse to these high inputs from the play synchronization flip-flops 54
34 and 55, thereby causing the reference moment flip-flop 64 to be reset by
35 the output V_{68} from the AND gate 68.

36 The moment the reference moment flip-flop 64 is thus reset is the

1 reference moment needed for play synchronization of the VTRs 1a and 1b
2 according to the instant invention. As the reference moment flip-flop 64
3 is reset as above, so will be the play synchronization flip-flops 54 and
4 55. Therefore, as indicated in FIG. 7, the play synchronization flip-flop
5 outputs V_{64} and V_{65} will go high only momentarily at t_2 . It will also
6 be noted from FIG. 7 that the NAND gate output V_{67} , AND gate output
7 V_{68} and NOR gate output V_{66} will all go low momentarily at t_2 . When
8 the series of vertical sync pulses V_{s1} and V_{s2} from both VTRs 1a and
9 1b are in phase with each other as in FIG. 7, the play synchronization
10 flip-flop output pulses V_{64} and V_{65} will be so short in duration that
11 they are not to affect the traveling speed of the cassette tapes 7a and
12 7b even though they are applied via the adders 56 and 57 to the cap-
13 stan motor driver circuits 24a and 24b, FIG. 4. Aside from these play
14 synchronization pulses of negligibly short durations, the driver circuits
15 24a and 24b will input the capstan motor servo signals by way of the
16 lines 45a and 45b, for causing the capstan motors 15a and 15b to be
17 driven accordingly.

18 Both vertical synch pulses V_{s1} and V_{s2} recur, of course, with a
19 cycle T_v in FIG. 7. What has happened from t_1 to t_2 , as explained
20 above, will repeat itself from t_3 to t_4 and so forth.

21 Let us now proceed to FIG. 8 for discussion of what occurs when
22 the vertical sync pulses V_{s1} from the first VTR 1a slightly lag in phase
23 from those V_{s2} from the second 1b, "slightly" because there is no time
24 spacing between every two associated sync pulses from both VTRs. The
25 play synchronization circuit 43 will then operate to bring the first VTR
26 1a into phase with the second 1b through the procedure set forth here-
27 inbelow.

28 It will be observed from FIG. 8 that, in this case, each of the
29 OR gate output pulses V_{65} has a duration, as from t_1 to t_3 , equal to
30 the sum of the duration, as from t_2 to t_3 , of one vertical sync pulse
31 V_{s1} from one VTR and the duration, as from t_1 to t_2 , of one associated
32 vertical sync pulse V_{s2} from the other VTR. Clocked by the leading
33 edge of each such OR gate output pulse V_{65} , the reference moment flip-
34 flop 64 will go high at t_1 , enabling the play synchronization flip-flops 54
35 and 55.

36 So enabled, the play synchronization flip-flop 55 will first go high

1 at t_2 when the NOT circuit 53 goes high in response to the trailing
2 edge of one vertical sync pulse V_{s2} from the second VTR. Then the
3 other play synchronization flip-flop 54 will go high at t_3 when the NOT
4 circuit 52 goes high in response to the trailing edge of the vertical sync
5 pulse V_{s1} from the first VTR 1a that immediately follows the pulse V_{s2} .
6 Both play synchronization flip-flops 54 and 55 being thus high at t_3 , the
7 NAND gate 67 will go low instantly, resetting the reference moment flip-
8 flop 64 via the AND gate 68.

9 The moment t_3 the reference moment flip-flop 64 is reset as
10 above is the reference moment in the case of FIG. 8, when both play
11 synchronization flip-flops 54 and 55 will also be reset. Their outputs
12 V_{64} and V_{65} are therefore shown to go low at t_3 . The play synchroni-
13 zation flip-flop 54 has now completed the production of a pulse of negli-
14 gibly short duration, whereas the other play synchronization flip-flop 55
15 has produced a pulse of much longer duration, lasting from t_2 to t_3 .

16 One cycle of operation of the play synchronization circuit 43, in
17 response to one vertical sync pulse V_{s1} from the first VTR and one as-
18 sociated similar pulse V_{s2} from the second VTR, has now been completed.
19 The next similar cycle will occur as the two associated vertical sync
20 pulses are input from t_4 to t_5 in FIG. 8.

21 Each FIG. 8 output pulse V_{64} of the play synchronization flip-flop
22 54 is too brief to take significant part in speed control of the magnetic
23 tape 7b, FIG. 2, in the second VTR 1b, just as the output pulses V_{64}
24 and V_{65} of both play synchronization flip-flop 54 and 55 were when both
25 series of vertical sync pulses V_{s1} and V_{s2} were in synchronism with each
26 other as in FIG. 7. It is the magnetic tape 7a in the first VTR 1a that
27 needs speed readjustment for synchronous driving with the tape 7b.

28 To that end, each output pulse V_{65} of the other play synchroniza-
29 tion flip-flop output 55 has its duration determined in proportion with the
30 phase difference between the two series of vertical sync pulses V_{s1} and
31 V_{s2} , to take active part in tape speed control in the first VTR 1a. The
32 adder 57, FIG. 5, of the play synchronization circuit 43 will add each
33 such play synchronization flip-flop output pulse and the capstan motor
34 servo signal fed from the capstan motor servo circuit 34a, FIG. 3, of the
35 first VTR controller 22a over the line 45a. The resulting output from
36 the adder 57 will be delivered to the capstan motor driver circuit 24a,

1 FIG. 4, of the first VTR 1a over the line 48a.

2 The capstan motor driver circuit 24a comprises an input selector
3 switch 69a and an amplifier 70a. The input selector switch 69a is shown
4 to have one fixed contact connected to the controller 22a, another fixed
5 contact connected to the VTR output 49a and thence to the play syn-
6 chronization circuit 43 by way of the line 48a, and a movable contact
7 for selectively connecting the two fixed contacts to the amplifier 70a.
8 FIG. 4 also shows the capstan motor driver circuit 24b of the second
9 VTR 1b, which is of like construction.

10 The input selector switch 69a is to choose the play synchroniza-
11 tion circuit 43 when the video player system is in play synchronization
12 mode, and the VTR controller 22a when it is not. The addition of the
13 capstan motor servo signal and the play synchronization signal is therefore
14 amplified and applied to the capstan motor 15a in play synchronization
15 mode, and only the capstan motor servo signal amplified and applied to
16 the capstan motor in non-play-synchronization mode. The same holds true
17 with the second VTR capstan motor driver circuit 24b.

18 Referring once again to FIG. 8, the play synchronization flip-flop
19 output pulse V_{55} that is produced right after each vertical sync pulse
20 V_{s2} will be combined with the capstan motor servo signal from the first
21 VTR controller 22a for joint delivery to the capstan motor driver circuit
22 24a. The first VTR capstan motor 15a will be accelerated during the t_2 -
23 t_3 duration of the play synchronization flip-flop output pulse V_{55} for
24 bringing the first tape 7a into phase with the second tape 7b.

25 Possibly, the delay of the first tape 7a may not be overcome by
26 the single output pulse V_{55} of the play synchronization flip flop 55.
27 Then a required number of such pulse will be produced, as from t_5 to
28 t_6 in FIG. 8, for reaccelerating the first VTR capstan motor 15a until
29 synchronism is attained between both series of vertical sync pulses from
30 the VTRs 1a and 1b as in FIG. 7. Normally, the vertical sync pulses are
31 recovered at a rate of one for each one sixtieth of a second, with er-
32 rors of no more than several percent. If there is an error of 2.5 per-
33 cent, for instance, then the time per field is as short as 0.000425 second.
34 Synchronism is therefore attainable with minimal speed readjustment of one
35 of the capstan motors 15a and 15b relative to the other.

36 It is also to be appreciated in connection with FIG. 8 that the

1 t_2-t_3 or t_5-t_6 duration of each play synchronization flip-flop output pulse
2 V_{55} is so determined as to coincide, and not to exceed, each vertical
3 retrace period of the video signal. The capstan motor 15a is therefore
4 readjusted in speed without affecting the picture being exhibited on the
5 screen.

6 In FIG. 9 are shown the vertical sync pulses V_{s2} from the second
7 VTR 1b lagging in phase from those V_{s1} from the first 1a, with a time
8 spacing between every two associated sync pulses from both VTRs. The
9 second VTR 1b is to be accelerated into phase with the first 1b in this
10 case, as will be detailed hereinbelow.

11 Inputting the two series of vertical sync pulses V_{s1} and V_{s2} , the
12 OR gate 65, FIG. 5, of the reference moment determination circuit 51 will
13 produce the output V_{65} composed of both series of vertical sync pulses.
14 First clocked at t_1 by the leading edge of one of the first series of
15 vertical sync pulses V_{s1} , the reference moment flip-flop 64 will go high
16 by taking in the NOR gate output V_{66} , enabling both play synchroniza-
17 tion flip-flops 54 and 55. Clocked at t_2 by the trailing edge of the
18 first vertical sync pulse V_{s1} , the first play synchronization flip-flop 54
19 will take in its data input and so go high at that moment. This high
20 output V_{54} will cause the NOR gate 66 to go low at t_2 .

21 Upon appearance of the associated one of the second series of
22 vertical sync pulses V_{s2} at t_3 , the OR gate 65 will again go high, clock-
23 ing the reference moment flip-flop 64. Its data input D being then low,
24 the reference moment flip-flop 64 will go low at t_3 , thereby resetting
25 both play synchronization flip-flops 54 and 55. One output pulse from
26 the play synchronization flip-flop 54 has now been terminated. The other
27 play synchronization flip-flop 55 will not respond to the trailing edge of
28 the vertical sync pulse V_{s2} appearing at t_3 , staying low.

29 The play synchronization flip-flop output V_{54} will be added by
30 the adder 56 to the capstan motor servo signal fed from the second VTR
31 controller 22b over the line 45b. The resulting adder output will be
32 delivered over the line 48b to the second VTR capstan motor driver cir-
33 cuit 24b, FIG. 4, in which the adder output will be directed by the
34 input selector switch 24b into the amplifier 70b preparatory to delivery
35 to the second VTR capstan motor 15b. This motor will then be acceler-
36 ated instantaneously to bring the lagging second VTR video tape 7b into

1 phase with the first VTR video tape 7a. If the second series of vertical
2 sync pulses V_{s2} does not come into synchronism with the first s_1 by the
3 single play synchronization pulse V_{s4} , the foregoing cycle of operation
4 from t_1 to t_3 will be repeated, as from t_4 to t_5 , until synchronization is
5 achieved.

6 The advantages gained by this first preferred embodiment of the
7 invention may be recapitulated as follows:

8 1. The two VTRs 1a and 1b can be compulsorily synchronized for
9 playback of the correlated recordings on the two video tapes 7a and 7b
10 by the external play synchronizer 3 of simple construction composed of
11 only the sync pulse separator circuits 42a and 42b and the play synchro-
12 nization circuit 43.

13 2. No dedicated reference signal is used; instead, a reference mo-
14 ment signal is produced from the vertical sync pulses from both VTRs in
15 order to produce in turn a play synchronization signal for accelerating
16 the capstan motor of the lagging VTR according to the phase difference
17 between the two series of vertical sync pulses. The circuitry of the
18 resulting play synchronizer is simpler and less expensive in configuration
19 than the prior art employing a dedicated reference signal source.

20 3. Capstan motor speed readjustment in response to a pulse or
21 pulses from either of the play synchronization flip-flops 54 and 55 is
22 made during vertical retrace, so that the pictures being displayed are not
23 affected in any way by the compulsory synchronization.

24 4. The play synchronization signals according to the invention are
25 combined with the standard capstan motor servo signals prior to delivery
26 to VTRs, in which selection is made by the input selector switches 24a
27 and 24b between the capstan motor servo signals alone and the combina-
28 tion of the play synchronization signals and capstan motor servo signals.
29 So constructed, the play synchronizer 3 lends itself to use as an external
30 adapter of commercially available VTRs.

31 5. Connected in circuit with the VTRs 1a and 1b, the play syn-
32 chronization circuit 43 will nevertheless operate only when the VTRs are
33 in condition for forced play synchronization, thanks to the provision of
34 the VTR status judgment circuit 50.

35

36

Second Form

The invention is herein applied to the three-VTR, three-display video player system shown in FIG. 10. The three VTRs 1a, 1b and 1c are of identical design, the third VTR 1c being similar to the VTRs 1a and 1b shown in FIG. 2, and so are the three displays 2a, 2b and 2c. The pertinent parts of the third VTR 1c will be identified by suffixing the letter c to the reference numerals used to denote the corresponding parts of the VTRs 1a and 1b. As in the first disclosed embodiment, the VTRs 1a-1c may be either independently coupled to the respective displays 2a-2c, as indicated by the solid lines in this figure, or to one display, as indicated by the dashed lines. At 3' is shown a play synchronizer according to the instant invention which is adapted for use with the three VTRs 1a-1c.

As depicted block-diagrammatically in FIG. 11, the modified play synchronizer 3' is broadly divisible into a first 42a, a second 42b and a third 42c vertical sync pulse separator circuit for deriving the vertical sync pulses from the composite video signals recovered from the tapes by the three VTRs 1a, 1b and 1c, respectively, and a play synchronization circuit 43' for creating play synchronization signals from the derived vertical sync pulses. The three vertical sync pulse separator circuits 42a-42c are of like configuration, the third circuit 42c being similar to the first two circuits 42a and 42b. Suffice it to say, therefore, that the third vertical sync pulse separator circuit 42c is connected to the video output terminal 26c and fourth controller output terminal 41c of the third VTR 1c for separating the vertical sync pulses V_{s3} from the third video output, and to the play synchronization circuit 3' for delivery of the vertical sync pulses thereto.

The play synchronization circuit 43' is designed on the same principles as the FIG. 5 play synchronization circuit 43 for production of capstan motor control signals, composed of play synchronization signals according to the invention and conventional capstan motor servo signals, which are applied to the three VTRs 1a-1c for their play synchronization. Toward this end the play synchronization circuit 43' is connected to the vertical sync pulse separator circuits 42a-42c by way of lines 44a-44c to the output terminals 38a, 39a, 49a and input terminal 49a of the first

1 VTR 1a, to the output terminals 38b, 39b and 40b and input terminal
2 49b of the second VTR 1b, and to the output terminals 38c, 39c and 40c
3 and input terminal 49c of the third VTR 1c. The terminals 26c, 38c-40c
4 and 49c of the third VTR 1c correspond to the terminals 26a, 38a-40a
5 and 49a of the first VTR 1a. Although the connection of the second
6 output line 48b of the play synchronization circuit 3 is not clearly indi-
7 cated in FIG. 11 for illustrative convenience, it is understood that the
8 output line 48b is connected to the terminal 49b of the second VTR 1b,
9 just as the output line 48b of the play synchronization circuit 43, FIG.
10 4, is shown connected to the terminal 49b of the second VTR.

11 As illustrated in more detail in FIG. 12, the play synchronization
12 circuit 3' comprises a third D flip-flop 70 for play synchronization in
13 addition to the two noted play synchronization flip-flops 54 and 55 of
14 the first embodiment, a third adder 88 in addition to the two noted ad-
15 ders 56 and 67, three AND gates 71, 72 and 73, a reference moment de-
16 termination circuit 51' which is an adaptation of the FIG. 5 reference
17 moment determination circuit 51 for use with three VTRs, three NOT cir-
18 cuits 81, 82 and 83, a three-input OR gate 84, and three AND gates 85,
19 86 and 87.

20 Instead of the VTR status judgment circuit 50, FIG. 5, of the first
21 disclosed play synchronization circuit 43, the modified synchronization cir-
22 cuit 43' has the three AND gates 71-73 having their inputs connected
23 respectively to the vertical sync pulse separator circuits 42a-42c by way
24 of the vertical sync pulse lines 44a-44c on the one hand and, on the
25 other, to the play command output terminals 39a-39c, FIG. 3, of the VTRs
26 1a-1c by way the lines 46a-46c. Thus are the vertical sync pulses V_{s1} -
27 V_{s3} allowed through the AND gates 71-73 only when high inputs indica-
28 tive of play commands are being input from the controllers of the VTRs
29 1a-1c. Any undesired operation of the play synchronization circuit 43',
30 triggered for instance by noise, is thus precluded when the VTRs 1a-1c
31 are in other than play mode.

32 The three play synchronization flip-flops 54, 55 and 70 have their
33 clock inputs T connected to the AND gates 71-73, respectively, their data
34 inputs D and preset inputs PR connected to a positive supply terminal
35 $+V$, and their reset inputs R to the reference moment determination cir-
36 cuit 51'.

1 The reference moment determination circuit 51' has three OR gates
2 74, 75 and 76 connected respectively to the *Q* outputs of the play syn-
3 chronization flip-flops 54, 55 and 70 on the one hand and, on the other,
4 to the play command lines 46a-46c via NOT circuits 78, 79 and 80. An
5 NAND gate 77, another component of the reference moment determination
6 circuit 51', have inputs connected to the three OR gates 74-76, and an
7 output connected as aforesaid to the reset inputs *R* of the play synchro-
8 nization flip-flops 54, 55 and 70. Alternatively, the OR gates 74-76 could
9 be coupled directly to the flip-flops 54, 55 and 70.

10 The OR gate 84 has its three inputs connected respectively to
11 the *Q* outputs of the play synchronization flip-flops 54, 55 and 70. The
12 output of this OR gate 84 is connected to all of the three-input AND
13 gates 85-87, the other inputs of which are connected respectively to the
14 *Q* outputs of the play synchronization flip-flops 54, 55 and 70 via the
15 NOT circuits 81-83, and to the play command lines 46a-46c. The AND
16 gates 85-87 could be connected directly to the inverting outputs of the
17 play synchronization flip-flops 54, 55 and 70.

18 The first adder 56 has one input connected to the capstan motor
19 servo line 45a of the first VTR 1a, another input to the AND gate 85,
20 and an output to the line 48a leading to the input terminal 49a of the
21 capstan motor driver circuit 24a, FIG. 4, of the first VTR. The second
22 adder 57 has one input connected to the capstan motor servo line 45b of
23 the second VTR 1b, another input to the AND gate 86, and an output to
24 the line 48b leading to the input terminal 49b of the capstan motor
25 driver circuit 24b of the second VTR. The third adder 88 has one in-
26 put connected to the capstan motor servo line 45c of the third VTR 1c,
27 another input to the AND gate 87, and an output to the line 48c leading
28 to the input terminal 49c of the capstan motor driver circuit of the third
29 VTR. Thus the adders 56-58 provide additions of the standard capstan
30 motor servo signals from the VTRs controllers and the play synchroniza-
31 tion signals from the AND gates 85-87, for delivery to the capstan motor
32 driver circuits of the VTRs 1a-1c.

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Operation of Second Form

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Reference may be had to the waveform diagrams of FIGS. 13-15

1 for the following discussion of the operation of the three-VTR video
2 player system of FIGS. 10-12. The following indicia will be used to de-
3 note the pertinent signals appearing in various parts of the FIG. 12 play
4 synchronization circuit 43' in the following operational description:

5 $V_{71} = V_{s1}$ = first series vertical sync pulses from the first verti-
6 cal sync pulse separator circuit 42a

7 $V_{72} = V_{s2}$ = second series of vertical sync pulses from the sec-
8 ond vertical sync pulse separator circuit 42b

9 $V_{73} = V_{s3}$ = third series of vertical sync pulses from the third
10 vertical sync pulse separator 42c

11 V_{54} = output from the first play synchronization flip-flop 54

12 V_{55} = output from the second play synchronization flip-flop 55

13 V_{70} = output from the third play synchronization flip flop 70

14 V_{74} = output from the first OR gate 74 of the reference moment
15 determination circuit 51'

16 V_{75} = output from the second OR gate 75 of the reference mo-
17 ment determination circuit 51'

18 V_{76} = output from the third OR gate 76 of the reference moment
19 determination circuit 51'

20 V_{77} = output from the NAND gate 77 of the reference moment
21 determination circuit 51'

22 V_{84} = output from the OR gate 84

23 V_{85} = output from the AND gate 85

24 V_{86} = output from the AND gate 86

25 V_{87} = output from the AND gate 87.

26 FIG. 13 represents the foregoing voltage signals when the three
27 series of vertical sync pulses V_{s1} , V_{s2} and V_{s3} from the three VTRs 1a,
28 1b and 1c are all in synchronism with one another; FIG. 14 the same
29 voltage signals when the sync pulses V_{s1} from the first VTR 1a are ad-
30 vanced in phase over those from the other VTRs 1b and 1c; and FIG. 15
31 the same voltage signals when the sync pulses V_{s3} from the third VTR
32 1c has a phase advance over those V_{s1} from the first 1a, with the sec-
33 ond VTR 1b being in stop mode.

34 The three play synchronization flip-flops 54, 55 and 70, FIG. 12,
35 of the play synchronization circuit 43' will all be clocked by the three
36 series of vertical sync pulses V_{s1} - V_{s3} if all the VTRs 1a-1c are in play

1 mode. Let us assume that all these series of vertical sync pulses are in
2 phase as in FIG. 13. The Q outputs V_{54} , V_{55} and V_{70} from the flip-
3 flops 54, 55 and 70 will all go high as at t_1 in FIG. 13 in response to
4 the leading edges of each vertical sync pulse of each series. These
5 high outputs from cause the three OR gates 74-76 of the reference mo-
6 ment determination circuit 51' go high, too, thereby making the NAND
7 gate 77 go low. The low output V_{77} will reset all the three flip-flops
8 54, 55 and 70 instantly after they have gone high at t_1 as above. As
9 the flip-flop outputs V_{54} , V_{55} and V_{70} become low again after the in-
10 stantaneous high state at t_1 , the output V_{77} from the reference moment
11 determination circuit 51' will become high again immediately after that
12 moment, enabling the flip-flops 54, 55 and 70.

13 The OR gate 84 will also respond to the instantaneous pulses from
14 all the flip-flops 54, 55 and 70, itself instantaneously going high at t_1 , as
15 indicated at V_{84} in FIG. 13. Although this instantaneous output pulse of
16 the OR gate 84 is applied to the three AND gates 85-87, these AND
17 gates will also input the inversions, by the NOT circuits 81-83, of the
18 flip-flop output pulses V_{54} , V_{55} and V_{70} at t_1 , so that the AND gate
19 outputs V_{85} - V_{87} will remain low.

20 No play synchronization pulses will thus be input to the adders
21 56-58. Directed from the three VTR controllers over the lines 45a-45c,
22 the capstan motor servo signals only will be fed over the play synchroni-
23 zation circuit output lines 48a-48c to the capstan motor driver circuits of
24 the three VTRs. No phase readjustment will occur in the VTRs in re-
25 sponse to the vertical sync pulses input to the phase synchronization cir-
26 cuit 43' from t_1 to t_2 .

27 The play synchronization circuit 43' will repeat the foregoing cycle
28 of operation in response to each set of three vertical sync pulses incom-
29 ing at the cycle T_v . No phase readjustment will occur, either, as long
30 as each such set of pulses remain in phase as in FIG. 13.

31 In FIG. 14 are shown the first series of vertical sync pulses V_{s1}
32 as having a phase advance over the other two series V_{s2} and V_{s3} ; the
33 second series of vertical sync pulses V_{s2} as having a phase lag from the
34 other two V_{s1} and V_{s3} ; and the third series of vertical sync pulses V_{s3}
35 as having a phase lag from the first V_{s1} and a phase advance over the
36 second V_{s2} . The first pulse of the first series of vertical sync pulses

1 V_{s1} is shown to appear from t_1 to t_2 , the first pulse of the second ser-
2 ies V_{s2} from t_4 to t_5 , and the first pulse of the third series V_{s3} from
3 t_2 to t_3 .

4 In that case, out of the three flip-flops 54, 55 and 70, the first
5 flip-flop 54 will first go high at t_1 in response to the leading edge of
6 one of the first series of vertical sync pulse V_{s1} . Then the third flip-
7 flop 70 will go high at t_2 in response to the leading edge of one of
8 the third series of vertical sync pulses V_{s3} . Finally, the second flip-flop
9 55 will go high at t_4 in response to the leading edge of one of the
10 second series of vertical sync pulses V_{s2} .

11 At t_4 , therefore, the three flip-flops 54, 55 and 70 will all be
12 high, making the NAND gate 77 of the reference moment determination
13 circuit 51' go low. All the flip-flops 54, 55 and 70 will in turn be re-
14 set by this low output from the circuit 51', themselves going low after
15 t_4 . Then the NAND gate 77 will go high again after having been mo-
16 mentarily low at t_4 and so enable the flip-flops 54, 55 and 70 for the
17 vertical sync pulses to be supplied subsequently.

18 A closer observation of FIG. 14 will reveal that the pulse thus
19 produced by the first flip-flop 54 rises at t_1 with the rise of one first
20 vertical sync pulse V_{s1} and decays at t_4 with the rise of one second
21 vertical sync pulse V_{s2} . The output pulse of the second flip-flop 55
22 rises and decays almost concurrently at t_4 . The output pulse of the
23 third flip-flop 70 rises at t_2 with the rise of one third vertical sync
24 pulse V_{s3} and decays also at t_4 .

25 In short the pulses issuing from the flip-flops 54, 55 and 70 dur-
26 ing the t_1 - t_4 period have durations equal to the time differences between
27 the leading edge, at t_4 (reference moment in this case), of one second
28 vertical sync pulses V_{s2} , which is the most delayed, and the leading
29 edges, at t_1 , t_4 and t_2 , respectively, of the three associated vertical sync
30 pulses V_{s1} - V_{s3} . Thus, as in the previous embodiment of the invention,
31 the reference moment determination circuit 51' functions to provide a ser-
32 ies of reference moments, and the flip-flops 54, 55 and 70 to ascertain
33 the phase departures of the three series of vertical sync pulses with
34 respect to the reference moments.

35 Inputting the three flip-flop outputs V_{54} , V_{55} and V_{70} , the OR
36 gate 84 will be high from t_1 to t_4 in FIG. 14. The inversions, by the

1 NOT circuits 81-83, of the flip-flop outputs V_{54} , V_{55} and V_{70} will be
2 allowed through the AND gates 85-87 only during the t_1 - t_4 period. The
3 resulting output from the first AND gate 85 will be low during this pe-
4 riod, so that no speed change of the capstan motor will be made for
5 synchronization purposes in the first VTR 1a, which is now assumed to
6 be most advanced in the phase of the vertical sync pulses. The capstan
7 motor of the first VTR 1a will, instead, be controlled solely by the cap-
8 stan motor servo signal fed from the first VTR controller.

9 Since the inversion of the second flip-flop output V_{55} during the
10 t_1 - t_4 period is high except at t_4 , the resulting output from the second
11 AND gate 86 will be high throughout the period. Added to the capstan
12 motor servo signal from the second VTR controller at the second adder
13 57, the high output from the second AND gate 86 will cause a corre-
14 sponding acceleration of the capstan motor of the second VTR 1b, which
15 is now assumed to be most delayed, in order to bring the second series
16 of vertical sync pulses V_{s2} into phase with the first V_{s1} .

17 The inversion of the third flip-flop output V_{70} is high from t_1 to
18 t_2 and low from t_2 to t_4 , the resulting output from the third AND gate
19 87 will be high from t_1 to t_2 . This third AND gate output V_{87} will be
20 added to the capstan motor servo signal from the third VTR controller at
21 the third adder 88 for delivery to the third VTR capstan motor driver
22 circuit. The third VTR capstan motor will be accelerated from t_1 to t_2
23 for bringing the third series of vertical sync pulses V_{s3} into phase with
24 the first V_{s1} .

25 The three VTRs 1a-1c may, or may not, be synchronized solely by
26 the foregoing cycle of operation taking place from t_1 to t_4 in FIG. 14.
27 The same cycle will be repeated as required after t_4 until synchronization
28 is achieved.

29 FIG. 15 has been drawn on the assumption that only the first and
30 third VTRs 1a and 1c are in play mode and that the first series of ver-
31 tical sync pulses V_{s1} lag in phase behind the third series of vertical
32 sync pulses V_{s3} . In this case the play synchronizer 3' is required to
33 accelerate the first VTR 1a into synchronism with the third 1c.

34 The third flip-flop 70 will go high upon appearance of one third
35 vertical sync pulse V_{s3} at t_1 , causing the third OR gate 76 of the ref-
36 erence moment determination circuit 51' to go high at that moment. The

1 first flip-flop 54 will go high upon appearance of one first vertical sync
2 pulse V_{s1} at t_3 , likewise causing the first OR gate 74 of the reference
3 moment determination circuit 51' to go high at that moment. Since the
4 second VTR 1b is now not in play mode, the second play command line
5 46b will be low, so that the NOT circuit 79 and therefore the second
6 OR gate 75 will both be high.

7 At t_3 , therefore, all the inputs to the NAND gate 77 of the ref-
8 erence moment determination circuit 51' will become high, causing the
9 NAND gate to go low. All the flip-flops 54, 55 and 70 will thus be
10 reset t_3 . The first and third flip-flops 54 and 70 will then go low,
11 whereas the second flip-flop 55 has been low. The OR gate 84 will
12 therefore be high from t_1 to t_3 , and so will be the AND gate 85. The
13 high output V_{85} from the AND gate 85 will be added by the adder 56
14 to the first VTR capstan motor servo signal, and the resulting adder out-
15 put delivered to the first VTR capstan motor driver circuit for accelerat-
16 ing the first VTR capstan motor. Here again the same cycle of operation
17 will be repeated after t_5 in FIG. 15 until the first 1a and the third 1c
18 VTRs become synchronized.

19 If, contrary to the showing of FIG. 15, the second VTR 1b were
20 in play mode, too, the second series of vertical sync pulses V_{s2} would
21 be allowed through the AND gate 72. Depending upon the phase rela-
22 tions of the second series of vertical sync pulses V_{s2} to the other two
23 series of such pulses V_{s1} and V_{s3} , they will undergo a different proce-
24 dure for synchronization therewith. Details of such a synchronization
25 procedure are considered self-evident from the foregoing description of
26 FIGS. 13-15.

27 It is now clear that the present invention is equally well applica-
28 ble to both two- and three-VTR display systems. In the case of the
29 three-VTR system of FIGS. 10-12, too, a reference moment is set up in
30 relation to the most delayed one of each set of three associated vertical
31 sync pulses. The phase relations of each set of vertical sync pulses
32 relative to the reference moment are determined by the flip-flops 54, 55
33 and 70, and capstan motor acceleration pulses are produced accordingly.
34 The three series of vertical sync pulses are forced into exact synchroni-
35 zation by use of simple and inexpensive electronics comprising the flip-
36 flops and logic circuits.

1 have their other inputs connected to the play command lines 46a-46c,
2 respectively. The other details of construction are as previously set
3 forth with reference to FIG. 12.

4 If the three series of vertical sync pulses V_{s1} - V_{s3} have the phase
5 relationship of FIG. 14, for instance, the outputs V_{54} and V_{70} from the
6 flip-flops 54 and 70 will be subtracted from the first and the third VTR
7 capstan motor servo signals on the lines 45a and 45c. The first and the
8 third VTR capstan motors will then be decelerated until the first and the
9 third series of vertical sync pulses V_{s1} and V_{s3} are delayed into phase
10 with the second V_{s2} which have been most delayed.

11 Fifth Form

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14 The adders 56 and 57 of FIG. 5 and adders 56, 57 and 88 of
15 FIG. 12 may all be each replaced by a signal selector circuit shown in
16 FIG. 18 and therein generally designated 90. The representative signal
17 selector circuit 90 is a simple combination of an on-off switch 91 and a
18 reverse-blocking diode 92. The switch 91 is connected between the cap-
19 stan motor servo line 45a, 45b or 45c and the play synchronization cir-
20 cuit output line 48a, 48b or 48c. Preferably a transistor or like elec-
21 tronic switch, the switch 91 is normally closed, opening in response to a
22 pulse on the play synchronization signal line 93, which in fact is the
23 output line of the flip-flop 54 or 55 in FIG. 5 or of the AND gate 85,
24 86 and 87 in FIG. 12. The play synchronization signal line 93 is con-
25 nected to the play synchronization circuit output line 48a, 48b or 48c
26 via the diode 92.

27 The capstan motor servo signal will travel freely through the sig-
28 nal selector circuit 90 when the play synchronization circuit 43 or 43' is
29 producing no pulses, for constant speed servo control of the associated
30 capstan motor. The switch 91 will open in response to, say, the t_2 - t_3
31 pulse V_{55} , FIG. 8, from the flip-flop 55, FIG. 5, so that only this pulse
32 will be allowed through the signal selector circuit 90 for accelerating the
33 second VTR capstan motor. In use of this signal selector circuit 90 the
34 voltage amplitude of the play synchronization pulses on the line 93 may
35 be made higher than the maximum voltage of the capstan motor servo
36 signal on the line 45a, 45b or 45c.

1 lowpass filters.

2 8. In the FIGS. 10-15 embodiment, as in the FIGS. 1-9 embodiment,
3 the vertical sync pulses V_{s1} - V_{s3} could be allowed through the AND gates
4 71, 72 and 73 only when the tape ends are not detected during operation
5 in play mode.

6 9. The invention could be applied to play synchronization of four
7 or more VTRs.

8 10. The invention could be applied to synchronization of various
9 videodisk players, in which application the speed of the videodisk drive
10 motor, or the readout speed of the buffer memory on the input side of
11 the digital-to-analog converter of the videodisk playback circuit, may be
12 controlled by the outputs from, for instance, the flip-flops 54, 55 and 70.

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